Center Independent Research & Development: GSFC IRAD

High-Rate Data Recorder

Completed Technology Project (2016 - 2020)

Project Introduction

Design a low cost, compact, solid-state data recorder for suborbital vehicles. The recorder will have a 45 GB minimum capacity and a record rate of at least 400 Mbps. Cost for recurring units will be nearly an eighth of the cost of commercial units with similar capabilities.

The circuit board central to this design will take in data from a bus that it masters. That bus will be parallel and likely implemented using a stack through connector. The board will packetize the data. It will then tag it with time and an indication of the device that sourced it. The board will also require a port for configuration and diagnostics amd may require an additional port to read the memory. The board will also have an interface for time stamping. That interface would be either IRIGB or GPS. If GPS is used, the data could eventually be tagged with position as well, but the position feature is not covered by this proposal.

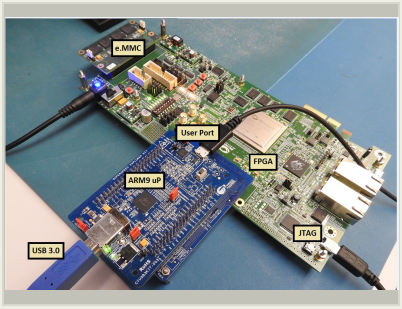
The backplane bus when initialized will wait for one or more external interface cards to request a time slice of bus access. The mainboard will acknowledge the highest priority interface card thereby allowing it to record at least one frame of tagged data before acknowledging the next interface. An additional future enhancement could allow multiple slower devices to record at the same time by splitting the backplane data path.

Anticipated Benefits

Recording data on a sounding rocket is desirable. It eliminates the need for redundant and more complicated ground assets. It also makes data that may have previously been deemed desirable but unobtainable seem conveniently accessible.

As the owner of this intellectual property NASA will benefit by controlling its growth and configuration. We will be less susceptible to changes in the marketplace and will also be able to take advantage of higher-speed memories as they become available.

Cost per unit will be dependent on the number of interface boards needed for a specific mission but it could be as low as $7K.



FPGA, USB3.0, & e.MMC

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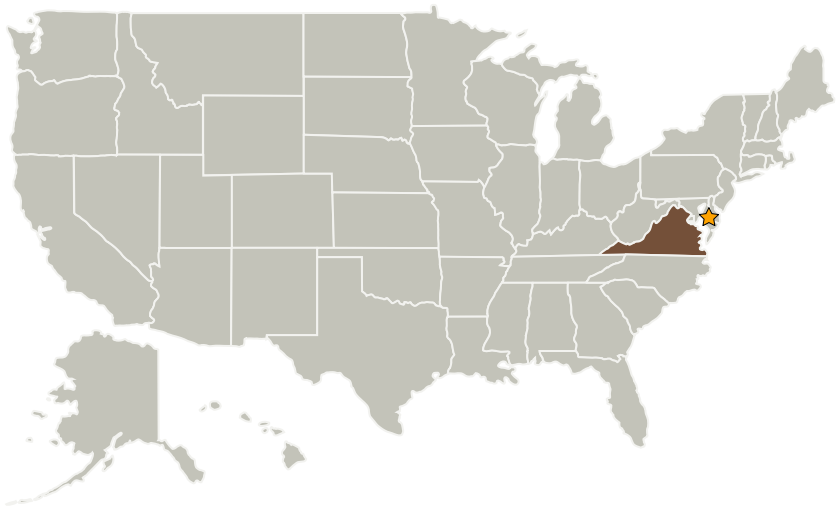
Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★Wallops Flight Facility(WFF)	Lead Organization	NASA Facility	Wallops Island, Virginia

Primary U.S. Work Locations
Virginia

Project Transitions

October 2016: Project Start

Organizational Responsibility

Responsible Mission Directorate:

Mission Support Directorate (MSD)

Lead Center / Facility:

Wallops Flight Facility (WFF)

Responsible Program:

Center Independent Research & Development: GSFC IRAD

Project Management

Program Manager:

Peter M Hughes

Project Managers:

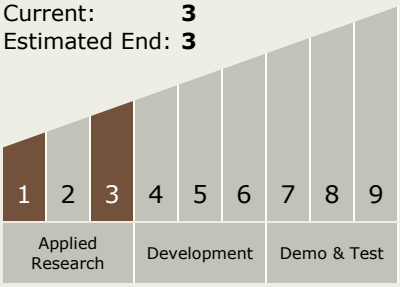
Daniel A Mullinix
Michael G Hitch

Principal Investigator:

Christopher F Lewis

Technology Maturity (TRL)

Start: **1**
Current: **3**
Estimated End: **3**



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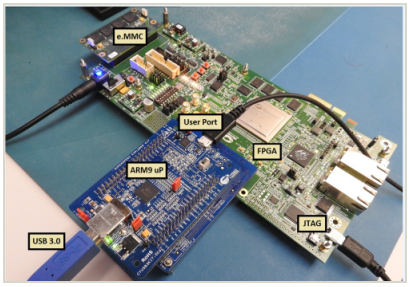
September 2020: Closed out

Closeout Summary: This effort has produced two populated circuit boards which have yet to be tested. Software was ported to the new environment and expanded upon considerably. Firmware is nearing completion as is the documentation explaining how to build and configure the device. The purpose of the Goddard Space Flight Center's Internal Research and Development (IRAD) program is to support new technology development and to address scientific challenges. Each year, Principal Investigators (PIs) submit IRAD proposals and compete for funding for their development projects. Goddard's IRAD program supports eight Lines of Business: Astrophysics; Communications and Navigation; Cross-Cutting Technology and Capabilities; Earth Science; Heliophysics; Planetary Science; Science Small Satellites Technology; and Suborbital Platforms and Range Services. Task progress is evaluated twice a year at the Mid-term IRAD review and the end of the year. When the funding period has ended, the PIs compete again for IRAD funding or seek new sources of development and research funding, or agree to external partnerships and collaborations. In some cases, when the development work has reached the appropriate Technology Readiness Level (TRL) level, the product is integrated into an actual NASA mission or used to support other government agencies. The technology may also be licensed out to the industry. The completion of a project does not necessarily indicate that the development work has stopped. The work could potentially continue in the future as a follow-on IRAD; or be used in collaboration or partnership with Academia, Industry, and other Government Agencies. If you are interested in partnering with NASA, see the TechPort Partnerships documentation available on the TechPort Help tab. http://techport.nasa.gov/help

Images



HdrRecorder
FPGA, USB3.0, & e.MMC
(https://techport.nasa.gov/image/40383)

Links

NASA Wallops Facebook
(https://www.facebook.com/NASAWFF)

Technology Areas

Primary:

- TX11 Software, Modeling, Simulation, and Information Processing
  - TX11.4 Information Processing
    - TX11.4.2 Intelligent Data Understanding

Target Destinations

Earth, Foundational Knowledge

NASA Wallops Twitter
(http://Www.twitter.com/nasa_wallops)

Project Website:

http://www.nasa.gov/centers/goddard/home/index.html